REMARKS/ARGUMENTS

New claims 63-65 have been added and claims 48, 55 and 62 have been amended to more clearly define the invention. Accordingly, claims 48-65 are pending in the application.

Claims 64 and 65 depend from claims 48 and 55 respectively. Claims 64 and 65 recite the limitation of "coupling said at least one polysilicon gate to a write row address line of said memory device." This limitation is not suggested by the references now of record and, for this and other reasons, claims 64 and 65 are believed to be in immediate condition for allowance.

Claims 48-62 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Office Action states that "incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor," is a method of using and intended use limitation. Claims 48, 55 and 62 have been amended to more clearly define the invention. The phrase "said memory device adapted to store information using said latchup of said multi-region planar thyristor," has been canceled from claims 48 and 55. The further phrase "incorporating said multi-region planar thyristor in a memory device," is a positive recitation of a step of a method of forming a circuit or device for storing information according to claims 48 and 55. Accordingly, the rejection of claim 48 under 35 U.S.C. § 112, second paragraph, is overcome.

The Office Action further indicates that the claim 55 recitation of " 'said gate adapted to receive a voltage for producing latch-up in said multi-region planar thyristor,' is an intended use recitation which does not further define the method of making the semiconductor device." In addressing the use of "adapted to" in patent claims, the court has noted that "[r]ather than being a mere direction of activities to take place in the future,

this language imparts a structural limitation..." In re Venezia 189 USPQ 149 (CCPA, 1976). Accordingly, to the extent that claim 55 includes the phrase "forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making the single junction a gated diode, said gate adapted to receive a voltage for producing latch up in said multi-region planar thyristor," claim 55 is believed to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Accordingly, the rejection of claim 55 under 35 U.S.C. § 112, second paragraph, is overcome.

As amended, claim 62 recites, "connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor and to a write row address line of a memory integrated circuit, said thyristor being adapted to transition from a first one to a second one of said at least two possible current states." This is a positive recitation of a step of a method of forming a circuit for storing information as one of at least two possible stable current states. Accordingly, the rejections of claims 48, 55 and 62 under 35 U.S.C. § 112, second paragraph, is believed to be overcome.

Claims 49-54 and 56-61 depend from claims 48 and 55 respectively and incorporate the respective limitations thereof. Accordingly, rejections of claims 49-54 and 56-61 under 35 U.S.C. § 112, second paragraph, are overcome for at least the reasons given above in relation to claims 48 and 55 respectively.

Claims 48-62 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over United States patent number 5,346,838 to Ueno (Ueno) in View of United States Patent Number 4,861,731 to Bhagat (Bhagat).

The present invention relates to a planar SRAM cell using bipolar latch-up and gated diode breakdown. Claim 48 recites:

A method of forming a circuit for storing information as one of at least two possible

stable current states, the method comprising the following steps: providing a semiconductor substrate; providing doped silicon regions to form a multi-region planar thyristor having at least four regions; forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor; and incorporating said multi-region planar thyristor in a memory device. (Emphasis added).

Ueno and Bhagat, taken alone or in combination, do not teach or suggest "incorporating said multi-region planar thyristor in a memory device," as claimed. Accordingly, the rejection of claim 48 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat is overcome, and allowance of claim 48 is in order.

Claims 49-54 each depend, directly or indirectly, from claim 48 and incorporate every limitation thereof. Accordingly, the rejections of claims 49-54 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat is overcome for at least the reasons given above the relation to claim 48, and allowance of claims 49-54 is in order.

Claim 55 recites:

A method of forming a device for storing information as one of at least two possible stable current states, the method comprising the following steps: providing a semiconductor substrate; providing doped silicon regions to form a multi-region planar thyristor having at least four regions; forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode, said gate adapted to receive a voltage for producing latch-up in said multi-region planar thyristor; and incorporating said multi-region planar thyristor in a memory device. (Emphasis added).

Ueno and Bhagat, taken alone or in combination, do not teach or suggest "[a]

method of forming a device for storing information as one of at least two possible stable current states, the method comprising ... incorporating said multi-region planar thyristor in a memory device." Accordingly, the rejection of claim 55 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat is overcome, and allowance of claim 55 is in order.

Claims 56-61 each depend, directly or indirectly, from claim 55 and incorporate every limitation thereof. Accordingly, the rejections of claims 56-61 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat is overcome for at least the reasons given above the relation to claim 55, and allowance of claims 56-61 is in order.

Claim 62 recites:

A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising: providing a semiconductor substrate; providing doped silicon regions to form a multi-region planar thyristor having at least four regions; forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; and connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor and to a write row address line of a memory integrated circuit, said thyristor being adapted to transition from a first one to a second one of said at least two possible current states. (Emphasis added).

Ueno and Bhagat , taken alone or in combination, do not teach or suggest "connecting said at least one polysilicon gate to... a write row address line of a memory integrated circuit." Accordingly, the rejection of claim 62 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat is overcome, and allowance of claim 62 is in order.

New claim 63 includes the limitation of "mutually coupling at least two gates of said plurality of gates to a write row address line of said memory integrated circuit," which is not taught or suggested in the references now of record. For this and other reasons, claim

63 is believed to be in immediate condition for allowance.

The attention of the Examiner is drawn to an Information Disclosure Statement submitted herewith. All claims now on the application are believed to be allowable over the references of record in this Application, whether taken alone or in combination.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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Version With Markings to Show Changes Made

Please rewrite claims 48, 55 and 62 as follows:

48. (Four Times Amended) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode;

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor; and

incorporating said multi-region planar thyristor in a memory device [, said memory device adapted to store information using said latchup of said multi-region planar thyristor].

55. (Twice Amended) A method of forming a device for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-

region planar thyristor thereby making said single junction a gated diode, said gate adapted to receive a voltage for producing latch-up in said multi-region planar thyristor; and

incorporating said multi-region planar thyristor in a memory device [, said memory device adapted to store information using said latchup of said multi-region planar thyristor].

62. (Once Amended) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; and

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor and to a write row address line of a memory integrated circuit, [whereby] said thyristor [transitions] being adapted to transition from a first one to a second one of said at least two possible current states.